In the Claims:

Please amend claims 1-8, 13-20, 27-29 and 31 as indicated below.

1. (Currently amended) An apparatus, comprising:

a memory;

a functional unit configured to perform a block operation on one or more block operands to generate a block result; and

a cache accumulator memory coupled to the memory and the functional unit, wherein the cache accumulator memory is configured to provide a block operand to the functional unit and to store the block result generated by the functional unit;

wherein the cache accumulator memory is configured to provide the block operand to the functional unit in response to receiving an instruction that uses an address in the memory to identify the block operand;

wherein the cache accumulator memory is configured as a cache of the memory; and

wherein the cache accumulator memory is configured to accumulate an intermediate result of a block accumulation operation performed on a given block operand, wherein the intermediate result is both a result of and an operand of the block accumulation operation.

2. (Currently amended) The apparatus of claim 1, wherein the cache accumulator memory comprises a dual-ported memory.

3. (Currently amended) The apparatus of claim 1, wherein the cache accumulator memory comprises at least two independently interfaced memory banks, wherein the cache accumulator memory is configured to provide the block operand from a first one of the independently interfaced memory banks and to store the block result in a second one of the independently interfaced memory banks.

4. (Currently amended) The apparatus of claim 1, wherein the cache accumulator memory is configured to indicate whether a particular block operand stored in the cache accumulator memory is modified with respect to a copy of that particular block operand in the memory.

5. (Currently amended) The apparatus of claim 1, wherein the cache accumulator memory is configured to load a copy of the block operand into the cache accumulator memory from the memory in response to the block operand not being present in the cache accumulator memory when the instruction is received.

6. (Currently amended) The apparatus of claim 5, wherein the cache accumulator memory comprises a plurality of block storage locations, wherein if all of the block storage locations are currently storing valid data, the cache accumulator memory is configured to select one of the block storage locations to overwrite with the copy of the block operand and to load the copy of the block operand into the selected one of the block storage locations.

7. (Currently amended) The apparatus of claim 6, wherein the cache accumulator memory is configured to use a least recently used algorithm to select the one of the block storage locations to overwrite.

8. (Currently amended) The apparatus of claim 6, wherein if data in the selected one of the block storage locations is modified with respect to a copy of that data in the memory, the cache accumulator memory is configured to write the data back to the

memory before loading the copy of the block operand into the selected one of the block storage locations.

9. (Original) The apparatus of claim 1, wherein the functional unit is configured to perform a parity calculation on the block operand.

10. (Original) The apparatus of claim 1, wherein the operation comprises a parity calculation, and wherein the command is issued by a storage system controller.

11. (Original) The apparatus of claim 10, wherein the functional unit is configured to calculate a parity block from a plurality of data blocks in a stripe of data, wherein the first block operand is a first one of the data blocks in the stripe of data.

12. (Original) The apparatus of claim 1, wherein the functional unit is configured to perform the operation on two block-operands.

13. (Currently amended) The apparatus of claim 12, wherein a first of the two block-operands is the block operand stored in the cache accumulator memory and a second of the two block-operands is provided on a data bus coupled to provide operands to the functional unit.

14. (Currently amended) The apparatus of claim 12, wherein a first of the two block-operands is the block operand stored in the cache accumulator memory and a second of the two block-operands is provided from the memory to the functional unit.

15. (Currently amended) The apparatus of claim 1, wherein the cache accumulator memory is configured to provide a word of the block operand to the functional unit during an access cycle in which the cache accumulator memory also stores a word of the block result generated by the functional unit.

16. (Currently amended) A method of performing a block accumulation operation, the method comprising:

receiving a first command to perform an operation on a first block operand identified by a first address in a memory;

in response to said receiving a first command:

loading the first block operand from the memory into a cache accumulator memory if the first block operand is not stored in the cache accumulator memory;

providing the first block operand from the cache accumulator memory to a functional unit; and

storing a block result of the operation generated by the functional unit into the cache accumulator memory;

wherein the cache accumulator memory is configured as a cache of the memory; and

wherein the cache accumulator memory is configured to accumulate an intermediate result of a block accumulation operation performed on a given block operand, wherein the intermediate result is both a result of and an operand of the block accumulation operation.

17. (Currently amended) The method of claim 16, wherein said providing comprises providing successive words of the first block operand and wherein said storing comprises storing successive words of the block result, wherein a word of the first block operand is provided from the cache accumulator memory to the functional unit during an

access cycle in which a word of the block result is stored in the cache accumulator memory.

18. (Currently amended) The method of claim 16, wherein the cache accumulator memory comprises a dual-ported memory, wherein said storing comprises overwriting the first block operand with the block result.

19. (Currently amended) The method of claim 16, wherein the cache accumulator memory comprises at least two independently interfaced memory banks, wherein said loading comprises loading the first block operand into a first one of the independently interfaced memory banks and wherein said storing comprises storing the block result in a second one of the independently interfaced memory banks.

20. (Currently amended) The method of claim 16, wherein the cache accumulator memory comprises a plurality of block storage locations, wherein if all of the block storage locations are currently storing valid data when the first command is received, said loading comprises selecting one of the block storage locations to overwrite with the copy of the first block operand and loading the copy of the first block operand into the selected one of the block storage locations.

21. (Original) The method of claim 20, wherein said selecting comprises using a least recently used algorithm to select the one of the block storage locations to overwrite.

22. (Original) The method of claim 20, further comprising writing data in the selected one of the block storage locations back to the memory if the data is modified with respect to a copy of that data in the memory.

23. (Original) The method of claim 16, further comprising the functional unit performing a parity calculation on the first block operand to generate the block result in response to said providing.

24. (Original) The method of claim 16, wherein the operation comprises a parity calculation, and wherein the command is issued by a storage system controller.

25. (Original) The method of claim 16, further comprising the functional unit performing the operation on the first block operand and a second block operand in response to said providing.

26. (Original) The method of claim 25, further comprising a data bus providing the second block operand to the functional unit.

27. (Currently amended) An apparatus, comprising:

means for storing data;

means for performing a block operation on one or more block operands to generate a block result; and

means for storing the block result generated by the means for performing the block operation and providing a block operand to the means for performing the block operation in response to an instruction that uses an address in the means for storing data to identify the block operand, wherein the means for storing the block result are coupled to the means for storing the block result and the means for performing a block operation;

wherein the means for storing the block result store a word of the block result during an access cycle in which the means for storing the block result provide a word of the block operand to the means for performing a block operation;

wherein the means for storing the block result is configured as a cache of the means for storing data; and

wherein the means for storing the block result is configured to accumulate an intermediate result of a block accumulation operation performed on a given block operand, wherein the intermediate result is both a result of and an operand of the block accumulation operation.

28. (Currently amended) A data processing system, comprising:

a host computer system;

a storage array;

an interconnect coupled to the host computer system and the storage array and configured to transfer data between the host computer system and the storage array; and

a parity calculation system configured to perform parity operations on data stored to the storage array, wherein the parity calculation system comprises a memory, a cache accumulator memory, and a parity calculation unit, wherein in response to an instruction using an address in the memory to identify the first block operand, the cache accumulator memory is configured to output a first block operand to the parity calculation unit and to store a first block result generated by the parity calculation unit;

wherein the cache accumulator memory is configured as a cache of the memory; and

wherein the cache accumulator memory is configured to accumulate an intermediate result of a block accumulation operation performed on a given block operand, wherein the intermediate result is both a result of and an operand of the block accumulation operation.

29. (Currently amended) The data processing system of claim 28, wherein the parity calculation unit is configured to perform a parity calculation on the first block operand provided by the cache accumulator memory and a second block operand provided on a data bus.

30. (Original) The data processing system of claim 29, wherein the parity calculation system is configured to calculate a parity block from a plurality of data blocks in a stripe of data, wherein the first block operand is a first one of the data blocks in the stripe of data and wherein the second block operand is a second one of the data blocks in the stripe of data.

31. (Currently amended) The data processing system of claim 28, wherein the cache accumulator memory is configured to store a word of the first block result during an access cycle in which the cache accumulator memory provides a word of the first block operand to the parity calculation unit.